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(5 AND 14).PGPB,USPT.	2
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DB=PGPB,USPT; PLUR=YES; OP=OR			
<a href="#"><u>L26</u></a>	l5 and l14	2	<a href="#"><u>L26</u></a>
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<a href="#"><u>L23</u></a>	l4 and l14	2	<a href="#"><u>L23</u></a>
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<a href="#"><u>L21</u></a>	l4 and l12	9	<a href="#"><u>L21</u></a>
<a href="#"><u>L20</u></a>	l3 and l14	2	<a href="#"><u>L20</u></a>
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<a href="#"><u>L18</u></a>	l3 and l12	13	<a href="#"><u>L18</u></a>
<a href="#"><u>L17</u></a>	l1 and l14	2	<a href="#"><u>L17</u></a>
<a href="#"><u>L16</u></a>	l1 and l13	9	<a href="#"><u>L16</u></a>

<u>L15</u>	L1 and l12	13	<u>L15</u>
<u>L14</u>	(718/101-108)![CCLS]	4266	<u>L14</u>
<u>L13</u>	(712/216-248)[CCLS]	6818	<u>L13</u>
<u>L12</u>	(712/2-300)[CCLS]	12167	<u>L12</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L11</u>	l5 and pipe\$7	30	<u>L11</u>
<u>L10</u>	l4 and pipe\$7	29	<u>L10</u>
<u>L9</u>	l3 and pipe\$7	40	<u>L9</u>
<u>L8</u>	l1 and pipe\$7	95	<u>L8</u>
<u>L7</u>	L3 and (reschedul\$6 or schedul\$6)	30	<u>L7</u>
<u>L6</u>	L1 and (reschedul\$6 or schedul\$6)	31	<u>L6</u>
<u>L5</u>	L1 and (schedul\$6)	31	<u>L5</u>
<u>L4</u>	L3 and (schedul\$6)	30	<u>L4</u>
<u>L3</u>	(flush\$5) near15 (stal\$5 or halt\$4 or held or hold\$3) near10 thread\$3 and (load\$3)	123	<u>L3</u>
<u>L2</u>	(flush\$5) near15 (stal\$5 or halt\$4 or held or hold\$3) near10 thread\$3 near25 (load\$3)	1	<u>L2</u>
<u>L1</u>	(flush\$5) near15 (stal\$5 or halt\$4 or held or hold\$3) near10 thread\$3	392	<u>L1</u>

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Oberg, J.; Ellerjee, P.;

*Euromicro Conference, 1998. Proceedings, 24th*

Volume 1, 25-27 Aug. 1998 Page(s):301 - 308 vol.1

Digital Object Identifier 10.1109/EURMIC.1998.711814

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Yong Meng Teo; Yew Kwong Ng;

*Simulation Symposium, 2002. Proceedings, 35th Annual*

14-18 April 2002 Page(s):245 - 252

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IEE CNF IEE Conference Proceeding

IEEE STO IEEE Standard

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Po-Yung Chang; Patt, Y.N.; Evers, M.;  
[Computer Architecture, 1996 23rd Annual International Symposium on](#)  
22-24 May 1996 Page(s):3 - 3  
Digital Object Identifier 10.1109/ISCA.1996.10012  
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2. **High-level automatic pipelining for sequential circuits**  
Marinescu, M.-C.V.; Rinard, M.;  
[System Synthesis, 2001. Proceedings. The 14th International Symposium on](#)  
2001 Page(s):215 - 220  
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3. **Improving branch prediction accuracy by reducing pattern history table interference**  
Po-Yung Chang; Evers, M.; Patt, Y.N.;  
[Parallel Architectures and Compilation Techniques, 1996. Proceedings of the 1996 Conference on](#)  
20-23 Oct. 1996 Page(s):48 - 57  
Digital Object Identifier 10.1109/PACT.1996.554029  
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